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Term	Documents
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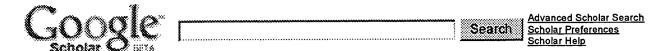
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DB=F	PGPB,USPT; PLUR=YES; OP=OR		
<u>L22</u>	12 and 120	6	<u>L22</u>
<u>L21</u>	12 and 118	15	<u>L21</u>
<u>L20</u>	(711/131,132)[CCLS]	351	<u>L20</u>
<u>L19</u>	(711/131-173)![CCLS]	19017	<u>L19</u>
<u>L18</u>	(711/131-173)[CCLS]	19017	<u>L18</u>
<u>L17</u>	L13 and l2	88	<u>L17</u>
<u>L16</u>	L15 and l2	12	<u>L16</u>
<u>L15</u>	L14 and l2	12	<u>L15</u>
<u>L14</u>	(712/200-203, 225,227)[CCLS]	793	<u>L14</u>
<u>L13</u>	(712/2-300)[CCLS]	12758	<u>L13</u>
DB=B	PGPB, USPT, USOC, EPAB, JPAB, DWPI, TDBD; PLUR=YES; OP=OR		

<u>L12</u>	(macro\$1 or macroinstruction\$1) near3 (push\$4 or pop\$4)	171	<u>L12</u>
<u>L11</u>	(macro\$1 or macroinstruction\$1) near15 (push\$4 or pop\$4) near12 tempor\$5	0	<u>L11</u>
<u>L10</u>	L9 not 15	12	<u>L10</u>
<u>L9</u>	L8 near25 register\$1	16	<u>L9</u>
<u>L8</u>	(macro\$1 or macroinstruction\$1) near3 (push\$4 or pop\$4)	171	<u>L8</u>
<u>L7</u>	L6 not 15	1	<u>L7</u>
<u>L6</u>	(macro\$1 or macroinstruction\$1) near25 (push\$4 or pop\$4) near15 (mov\$3 or transfer\$4) near25 register\$1	8	<u>L6</u>
<u>L5</u>	(macro\$1 or macroinstruction\$1) near15 (push\$4 or pop\$4) near15 (mov\$3 or transfer\$4) near15 register\$1	7	<u>L5</u>
<u>L4</u>	(macro\$1 or macroinstruction\$1) near12 (push\$4 or pop\$4) near15 (mov\$3 or transfer\$4) near12 register\$1	7	<u>L4</u>
<u>L3</u>	(macro\$1 or macroinstruction\$1) near6 (push\$4 or pop\$4) near15 (mov\$3 or transfer\$4) near12 register\$1	7	<u>L3</u>
<u>L2</u>	(macro\$1 or macroinstruction\$1) near6 (push\$4 or pop\$4 or move)	918	<u>L2</u>
T.1	(macro\$1 or macroinstruction\$1) near15 (push\$4 or pop\$4 or move)	1336	L1

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All Results

E CLARKE

B Holmer

J Stichnoth

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[PS] Realization of PRAMs: Processor Design - group of 5 »

J Keller, WJ Paul, D Scheerer - Proc. WDAG94, 8th Int. Workshop on Distributed Algorithms,

..., 1994 - pv.fernuni-hagen.de

... Push and pop instructions allow ... Therefore the register RAM's have to be either

dual{ported or one has to use two single{ port RAM's and partition the ...

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BK Holmer, B Sano, M Carlton, P Van Roy, R Haygood ... - Computer Architecture, 1990.

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JM Stichnoth, GY Lueh, M Cierniak - Proceedings of the ACM SIGPLAN 1999 conference on

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... bit to indicate whether it is a single instruction (and ... pointer, it is because of

a push, pop, or call ... we must record the number of macro-instruction records ... Cited by 35 - Related Articles - Web Search - Bl. Direct

CalmRISC TM-32: a 32-bit low-power MCU core - group of 7 »

S Cho, S Park, S Kim, Y Kim, SW Jeong, BY Chung, ... - ASICs, 2000. AP-ASIC 2000.

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... pushq and popq are used to push or pop four registers in sequence ... In our first

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implementation, these datapath macro blocks were compiled, and all the ...

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... ten SPUR local registers are used as temporaries by the macro-expansion code. ... better performance than the PLM for programs that push and pop choice points ...

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DW Jones - ACM SIGARCH Computer Architecture News, 1988 - portal.acm.org ... MACRO PUSHO CODE DUP CODE DUP CODE SUB ENDMAC ... PUSH ptr ; ptr CODE DUP; ptr CODE

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Using a Java Optimized Processor in a Real World Application - group of 3 » M Schoeberl - Proceedings of the First Workshop on Intelligent Solutions ... - jopdesign.com ... respect to stack manipulation in pop or push: Pop instructions reduce ... operand or for stack spill on push instructions and ... a reset signal to a 32 macro-cell PLD ... Cited by 5 - Related Articles - View as HTML - Web Search

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